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10/805,915	03/22/2004	Stephen Wu	BP3088	9674

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EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,915	WU, STEPHEN	
	Examiner	Art Unit	
	Naheed Ejaz	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14* is/are allowed.

6)☒ Claim(s) *1,6-9,15,19 and 20* is/are rejected.

7)☒ Claim(s) *2-5 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 8, 9 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al. (2002/0011896) in views of Hayashi et al. (2002/0008572), as applied to claim 15 below, and Adachi (5,272,452), and further in view of Shawhan (4,019,148).

3. As per claim 1, Yokoyama teaches, 'a PFD (Phase/Frequency Detector) that is operably coupled to determine a phase difference between transitions of a feedback signal and an input signal' (figure 1, element 52, page # 3, paragraph # 0026) (it is noted that Yokoyama is not only using the circuitry that includes phase detector 52 (figure 1) in order to generate a reference signal (clock signal) (page # 2, paragraph # 0024, lines 6-8) but also detecting frequency in order to adjust the center frequency of the gm-C filter 11 (band pass filter) (figure 1, page # 2, paragraph # 0024, lines 1-6) which is considered to be equivalent to the claim limitations of having 'a PFD (Phase/Frequency Detector)), 'a CP (Charge Pump) operably coupled to convert the phase difference into a charge pump current (figure 1, element 53, page # 3, paragraph # 0026); a loop filter operably coupled to convert the charge pump current into a VCO (Voltage Controlled Oscillator) control voltage (figure 1, element 54); a VCO (Voltage

Controlled Oscillator) (figure 1, element 55) operably coupled to convert the VCO control voltage into a recovered clock , wherein the feedback signal is derived from the recovered clock (figure 1, element 55 & 'reference signal', page # 2, paragraph # 0024)

Yokoyama do not teach amplitude detector.

Hayashi teaches, 'the VCO includes a plurality of g_m (transconductance) cells (figure 1, elements 3 and 3a); an amplitude detector that detects an amplitude of the recovered clock and that biases the plurality of g_m cells of the VCO such that the each g_m cell of the plurality of g_m cells operates substantially within its linear operating region (see claim 15 rejection above).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Hayashi into Yokoyama in order to realize different states of oscillation (diverged or attenuated) while keeping the amplitude constant thus provide a g_m-C filter system having low power consumption as taught by Hayashi (page # 1, paragraph # 0006 & page # 3, paragraph # 0027, lines, 12-19).

Yokoyama and Hayashi do not teach series connection of resistor and capacitor.

Adachi teaches 'the loop filter is implemented as a LPF (Low Pass Filter) having a resistor and a capacitor connected in series such that the capacitor is shunted to ground' (see claim 19 rejection below)

It would have been obvious to one of ordinary skill in the art, at the time invention was made to implement the teachings of Adachi into Yokoyama and Hayashi in order to provide a PLL circuit capable of changing over at high speed with small fluctuations of

frequency when the bandwidth of the loop filter is change over in a simple constitution (col.1, lines 34-38) as taught by Adachi.

Yokoyama, Hayashi and Adachi do not teach selection of band pass filter control voltage from a node that connects the resistor and the capacitor.

Shawhan teaches, 'a BPF (Band Pass Filter) control voltage is selected from a node that connects the resistor and the capacitor; and wherein the BPF control voltage determines a tuning frequency of a BPF to which the PLL is communicatively coupled' (see claim 19 rejection below).

It would have been obvious to one of ordinary skill in the art, at the time of invention was made, to implement the teachings of Shawhan into Yokoyama, Hayashi & Adachi in order to insure proper phasing of the switching signal produced by a phase-locked-loop as taught by Shawhan (col.5, lines 40-43) thereby providing a higher degree of noise rejection (col.1, lines 56-61).

4. As per claim 8, Yokoyama discloses, 'the BPF control voltage is a continuous time analog voltage signal' (figure 1, elements 11 & 40, page # 2, paragraph # 0025) (it is noted that gm-C filter 11 (figure 1) is band pass filter (page # 2, paragraph # 0023, lines 3-5)).

5. As per claim 9, Yokoyama teaches, 'the PLL is implemented within an AFE (Analog Front End) of a communication device' (figure 9, elements 60 & 71, page # 5, paragraphs # 0056 & 0057), 'the communication device is a transceiver or a receiver' (page # 1, paragraph # 0010).

6. As per claim 19, Yokoyama and Hayashi teach all the limitations in the previous claims on which claim 19 depends but they fail to disclose series connection of resistor and capacitor.

Adachi teaches a loop filter to form a phase lock loop having a resistor and capacitor connected in series and they are shunted to ground (figure 1, Abstract, col.1, lines 39-52) which reads on claim limitations 'the loop filter of the PLL is implemented as a LPF (Low Pass Filter) having a resistor and a capacitor connected in series such that the capacitor is shunted to ground'.

It would have been obvious to one of ordinary skill in the art, at the time invention was made to implement the teachings of Adachi into Yokoyama and Hayashi in order to provide a PLL circuit capable of changing over at high speed with small fluctuations of frequency when the bandwidth of the loop filter is change over in a simple constitution (col.1, lines 34-38) as taught by Adachi.

Yokoyama, Hayashi & Adachi do not teach band pass filter control voltage from a node that connects the resistor and the capacitor.

Shawhan teaches a band pass filter control voltage from a node that connects the resistor and the capacitor (figure 4, elements 172 & 174, col.5, lines 19-31).

It would have been obvious to one of ordinary skill in the art, at the time of invention was made, to implement the teachings of Shawhan into Yokoyama, Hayashi & Adachi in order to insure proper phasing of the switching signal produced by a phase-locked-loop as taught by Shawhan (col.5, lines 40-43) thereby providing a higher degree of noise rejection (col.1, lines 56-61).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al. (2002/0011896) in views of Hayashi et al. (2002/0008572), Adachi (5,272,452), and Shawhan (4,019,148), as applied to claim 1 above, and further in view of Kobayashi (5,550,520).

10. As per claim 6, Yokoyama, Hayashi, Adachi and Shawhan teach all the limitations in the previous claim on which claim 6 depends but they fail to disclose the input signal to PFD (phase/frequency detector) has substantially a center frequency of the BPF.

Kobayashi teaches input signal to phase frequency detector 72 (Figure 4, element 72) which has substantially a center frequency of band pass filter 10 (figures 3 & 4, col.5, lines 50-63).

It would have been obvious to one of ordinary skill in the art, at the time of invention was made, to implement the teachings of Kobayashi into Yokoyama, Hayashi, Adachi & Shawhan in order to adjust the bias voltages to maintain a zero dB pass band insertion loss and a stable center frequency of the filter as taught by Kobayashi (col.5, lines 59-63) thus compensate for resistive losses (col.1, lines 62-65).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al. (2002/0011896) in views of Hayashi et al. (2002/0008572), Adachi (5,272,452) and Shawhan (4,019,148), as applied to claims 1 & 15 above, and further in view of Reinhardt et al. (6,198,354) (hereinafter, Reinhardt).

9. As per claim 7, Yokoyama, Hayashi, Adachi and Shawhan teach all the limitations in the previous claims on which claim 7 depends but they fail to disclose elimination of spur or glitch content within band pass filter.

Reinhardt teaches, 'the loop filter of the PLL substantially eliminates any spur or glitch content within the BPF control voltage' (see figure 2, elements 30, 40 & 42, col.4, lines 8-20).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Reinhardt into Yokoyama, Hayashi, Adachi & Shawhan in order to produce desired phase lock loop bandwidth characteristics by eliminating spur from phase frequency detector as taught by Reinhardt (col.4, lines 13-17).

10. Claims 15 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al. (2002/0011896) in view of Hayashi et al. (2002/0008572) (hereinafter, Yokoyama and Hayashi respectively).

11. As per claim 15, Yokoyama teaches, 'oscillating a VCO (Voltage Controlled Oscillator) (figure 1, element 55) of a PLL (Phase Locked Loop) (figure 1, element 50) at a center frequency of a BPF (Band Pass Filter) (figure 1, element 11, page # 2, paragraph # 023, lines 3-10), wherein the PLL is communicatively coupled to the BPF (figure 1, elements 50 & 11); selecting an BPF control voltage from a loop filter of the PLL' (figure 1, elements 50, 54, 55 & 11, page # 2, paragraphs # 0024 & 0025, page # 3, paragraph # 0026) (it is noted that in the mentioned paragraphs Yokoyama is adjusting the center frequency of the gm-C filter 11 (BPF) based on the reference signal

from PLL circuit 50 (page # 2, paragraph # 0024, lines 20-30 & paragraph # 0025) which is generated using low pass filter 54 values as well (page # 3, paragraph # 0026) hence reads on claim limitations of selection of BPF control voltage from a loop filter of PLL), 'providing the selected BPF control voltage from the loop filter of the PLL to the BPF thereby tuning the BPF to operate at its center frequency' (figure 1, elements 11, 30, 50 & 54, page # 2, paragraphs # 0024 & 0025, page # 3, paragraph # 0026).

Yokoyama does not adjust amplitude of an output of the VCO.

Hayashi discloses, 'adjusting an amplitude of an output of the VCO to ensure that each g_m (transconductance) cell of a plurality of g_m cells of the VCO operates within its respective linear region' (see figure 2, elements 1a, 3 & figures 3A-3C, page # 1, paragraph # 0002, page # 3, paragraphs # 0027 & 0028) (it is noted that Hayashi is adjusting the output resistance value of the g_m amplifier 3a with respect to a value defined between the output resistance value obtained when the oscillation is diverged and the output resistance value obtained when the oscillation is attenuated (page # 3, paragraph # 0027, lines 19-23) so that the g_m cells of VCO would operate in certain region which is linear).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Hayashi into Yokoyama in order to realize different states of oscillation (diverged or attenuated) while keeping the amplitude constant thus provide a g_m–C filter system having low power consumption as taught by Hayashi (page # 1, paragraph # 0006 & page # 3, paragraph # 0027, lines, 12-19).

12. As per claim 20, Yokoyama teaches a high-precision filter tuning control system which is applicable to the receiver section of a cell phone (page # 1, paragraph # 0010) which is equivalent to the claim limitations of 'the method is performed within a communication device; and the communication device is a transceiver or a receiver'.

Allowable Subject Matter

13. Claims 2-5 & 16-18 are objected to as being dependent upon a rejected base claims, claims 1 & 15 respectively, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 10-14 are allowed. The following is a statement of reasons for the indication of allowable subject matter:

15. As per claims 10-14: the prior art of record fails to teach or suggest A PLL (phase locked loop) implemented to perform high precision continuous time BPF (Band Pass Filter) tuning, the PLL comprising: wherein the BPF is implemented as a g_m C (transconductance-capacitance) filter that includes at least one additional plurality of g_m cells; wherein the plurality of g_m cells of the VCO and the ate least one additional plurality of g_m cells of the g_m C filter both include substantially identical g_m cells as recited in claim 10 in combination with other elements in the claim.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hwang (5,534,943) teaches frequency modulation system having control of a carrier frequency (see col.4, lines 6-33).

Contact Information

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Naheed Ejaz
Examiner
Art Unit 2611

NE.
4/25/2007

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